What is claimed is:

1. A computer system comprising:

at least one main processor;

a sub processor connected to an input/output unit which is operated by an operator; and

a crossbar switch, connected to said at least one main processor and said sub processor, for transferring data between said main processor and said sub processor, said crossbar switch including a diagnosis section which diagnoses a failure in said main processor in accordance with a command input from said input/output unit and given to said sub processor,

said diagnosis section being capable of receiving data to be transmitted to said main processor from said input/output unit via said sub processor and causing said main processor to read said data, and receiving data to be transmitted to said input/output unit from said main processor and transmitting said data to said input/output unit via said sub processor.

2. The computer system according to claim 1, wherein said diagnosis section includes a serial controller having a first memory section where data to be transmitted to said input/output unit from said at least one main processor is written by said main processor, and a second memory section where data to be transmitted to said main processor from said input/output unit is written by said sub processor.

3. The computer system according to claim 2, wherein allocated to said serial controller are a first address for allowing said at least one main processor to write data in said first memory section and a second address for allowing said sub processor to write data in said second memory section.

4. The computer system according to claim 3, wherein said serial controller

gives an instruction to read a memory content from said first memory section to said sub processor when data is written in said first memory section by said at least one

main processor, and

gives a permission for interruption to said sub processor when a request to write data into said second memory section has been made by said sub processor and is interruptible.

5. The computer system according to claim 4, wherein said diagnosis section further includes at least one register which stores data representing a result of a failure diagnosis, and

said sub processor reads said data representing said result of said failure diagnosis from said register in accordance with an instruction given from said input/output unit and sends said read data to said input/output unit.

6. The computer system according to claim 4, wherein said diagnosis section includes a plurality of serial controllers respectively corresponding to a plurality of main processors, and

said sub processor writes data to be transmitted to one of said plurality of main processors, which is input from said input/output unit, in said second memory section of that serial controller which corresponds to said main processor where said data is to be transmitted by designating an address of that serial controller.

7. The computer system according to claim 6, wherein said input/output unit gives an instruction to said sub processor, allows said sub processor to execute a process based on said instruction, receives data representing a result of said process from said sub processor, gives an instruction to said at least one main processor via said sub processor and said diagnosis section, allows said main processor to execute a process based on that instruction, receives data representing a result of that process via said diagnosis section and said sub processor section, said input/output unit serves as a common console for said sub processor and said main processor.

8. A data processing method for use in a computer system comprising at least one main processor, a sub processor connected to an input/output unit which is operated by an

operator, and a diagnosis section which is connected to said main processor and said sub processor and diagnoses a failure in said main processor together with said sub processor in accordance with a command given from said input/output unit, said method comprising the steps of:

transmitting first data to be transmitted to said at least one main processor to said sub processor from said input/output unit, allowing said sub processor to store said transmitted first data in said diagnosis section, allowing said main processor to read said first data stored in said diagnosis section and allowing said main processor to execute a process based on said read-out first data; and

allowing said main processor to store second data to be transmitted to said input/output unit in said diagnosis section, allowing said sub processor to read said stored second data from said diagnosis section and transmit said second data to said input/output unit and allowing said input/output unit to display contents of said transmitted second data.

9. The data processing method according to claim 8, wherein said diagnosis section includes a serial controller having a first memory section for storing said first data to be transmitted to said input/output unit from said at least one main processor, and a second memory section for storing said second data to be transmitted to said main processor from said input/output unit, and

a first address which is designated by said at least one main processor and a second address which is designated by said sub processor are allocated to said serial controller.

10. The data processing method according to claim 9, wherein serial controllers respectively corresponding to plurality of main processors are provided in said diagnosis section, said sub processor stores said second data to be transmitted to one of said plurality of main processors in that serial controller which corresponds to said main processor where said second data is to be transmitted, and said main processor where said second data is to be transmitted reads said second data stored in that serial controller and executes a process based on said second data.